

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:

ARASH HASSIBI, ET AL.

Application No.: 09/843,486

Filed: April 25, 2001

For: **Optimal Simultaneous Design and
Floorplanning of Integrated Circuit**

Art Group: 2811

Examiner: Quang D. Vu

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97

Commissioner for Patents
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Alexandria, VA 22313-1450

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Respectfully submitted,

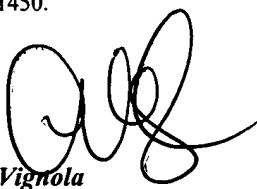
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Robert B. O'Rourke, Reg. No. 46,972

Date: 9/1/09

12400 Wilshire Boulevard, 7th Floor
Los Angeles, CA 90025
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Sheet 1 of 4 Attorney Docket Number 004363.P004

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (If known)				
		US-	6,578,179 B2	06-10-2003	Shirotori, et al.	
		US-	6,574,786 B1	06-03-2003	Pohlenz, et al.	
		US-	6,539,533 B1	03-25-2003	Brown, III et al.	
		US-	6,581,188	06-17-2003	Hosomi, et al.	
		US-	6,311,315	10-30-2001	Tamaki	
		US-	6,002,860	12-14-1999	Voinigescu, et al.	
		US-	5,754,826	05-19-1998	Gamal, et al.	
		US-	5,633,807	05-27-1997	Fishburn, et al.	
		US-	5,055,716	10-08-1991	El Gamel	
		US-	5,289,021	02-22-1994	El Gamel	
		US-	4,827,428	05-02-1989	Dunlop, et al.	
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FOREIGN PATENT DOCUMENTS

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		Country Code ³	Number ⁴ Kind Code ⁵ (if known)				
		WO	01/37429 A1	05-25-2001	HORAN, et al.		

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		Application Number	09/843,486
		Filing Date	4-25-01
		First Named Inventor:	Arash Hassibi, et al.
		Art Unit	2811
		Examiner Name	Quang D. Vu
		Attorney Docket Number	004363.P004
Sheet	2	of	4

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		HERSHENSON, M., et al., "Automated Design of Folded-Cascode Op-Amps with Sensitivity Analysis", pp. 121-124, Electronics, Circuits and Systems, IEEE International Conference on LISBOA, September 7-10, 1998.	
		HERSHENSON, M., et al., "GPCAD: A Tool for CMOS Op-Amp Synthesis" 8 pages, Proceedings of the IEEE/ACM International Conference on Computer Aided Design (ICCAD), pp. 296-303, November 1998.	
		HERSHENSON, M., et al., "Posynomial models for MOSFETs" 9 pages, July 7, 1998.	
		CHANG, H, et al., "A Top-Down, Constraint-Driven Design Methodology for Analog Integrated Circuits" 6 pages, IEEE 1992 Custom Integrated Circuits Conference.	
		CHAVEZ, J., et al, "Analog Design Optimization: A Case Study" 3 pages, IEEE, January 1993.	
		KORTANEK, K.O., et al., "An Infeasible interior-point algorithm for solving primal and dual geometric programs" pp. 155-181, Mathematical Programming 76 (1996).	
		GEILEN, G., et al., "Analog Circuit Design Optimization Based on Symbolic Simulation and Simulated Annealing", pp. 707-713, IEEE Journal of Solid-State Circuits, Vol. 25, No. 3, June 1990.	
		FISHBURN, J, et al., "TILOS: A Posynomial Programming Approach to Transistor Sizing" pp. 326-328, IEEE, 1985.	
		MAULIK, P., et al., "Integer Programming Based on Topology Selection of Cell-Level Analog Circuits", 12 pages, IEEE Transactions On Computer-Aided Design Of Integrated Circuits And Systems, Vol. 14, No. 4, April 1995.	
		SWINGS, K., et al., "An Intelligent Analog IC Design System Based On Manipulation Of Design Equations" pp. 8.6.1- 8.6.4, IEEE 1990, Custom Integrated Circuits Conference.	
		NESTEROV, Y., et al., "Interior-Point Polynomial algorithms in Convex Programming" 8 pgs., 1994, Society for Industrial and Applied mathematics.	

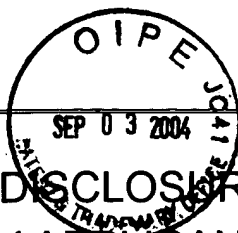
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		YANG, H.Z., et al., "Simulated Annealing Algorithm with Multi-Molecule: an Approach to Analog Synthesis" pp. 571-575, IEEE, 1996,			
		WONG, D.F., et al., "Simulated Annealing For VLSI Design" 6 pages, 1998, Kulwer Academic Publishers.			
		MAULIK, P., et al., "Sizing of Cell-Level Analog Circuits Using Constrained Optimization Techniques" pp. 233-241, IEEE Journal of Solid-State Circuits, Vol. 28, No. 3, March 1993.			
		OCHOTTA, E, et al., "Synthesis of High -Performance Analog Circuits in ASTRX/OBLS" pp. 273-295, IEEE Transactions on Computer-Aided Design of Integrated Circuits And Systems, Vol. 15, No. 3, March 1996.			
		WRIGHT, S., "Primal-Dual Interior-Point Methods" pp. 1-3, http://www.siam.org/books/wright , Printed August 19, 1998			
		SHYU, J., et al., "Optimization-Based Transistor Sizing" pp. 400-408, IEEE Journal of Solid-State Circuits, Vol. 23, No. 2, April 1998.			
		WRIGHT, S., "Primal-Dual Interior-Point Methods" 14 pages, 1997, Society for Industrial and Applied Mathematics.			
		VAN LAARHOVEN, P.J.M., et al., "Simulated Annealing: Theory and Applications" 26 pages, 1987, Kulwer Academic Publishers.			
		HERSHENSON, M., et al., "CMOS Operational Amplifier Design and Optimization via Geometric Programming" pp. 1-4, Analog Integrated Circuits, Stanford University.			
		AGUIRRE, M.A., et al., "Analog Design Optimization by means of a Tabu Search Approach" pp. 375-378.			
		MEDEIRO, F., et al., "A Statistical Optimization-Based Approach for Automated Sizing of Analog Cells", pp. 594-597, Dept. of Analog Circuit Desing.			

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NON PATENT LITERATURE DOCUMENTS				
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		SPATNEKAR, S., "Wire Sizing as a Convex Optimization Problem: Exploring the Area-Delay Tradeoff" 27 pages, Dept. of Electrical and Computer Engineering.		
		SU, H., et al., "Statistical Constrained Optimization of Analog MOS Circuits Using Empirical Performance Models" pp. 133-136.		
		VASSILIOU, I., et al, "A Video Driver System Designed Using a Top-Down, Constraint-Driven Methodology" 6 pages.		
		SAPATNEKAR, S, et al., "An Exact Solution to the Transistor Sizing Problem for CMOS Circuits Using Convex Optimization" 35 pages.		

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